TS32MMQ64V5M

214PIN DDR2 533 Micro-DIMM
256MB With 32Mx16 CL4

Description

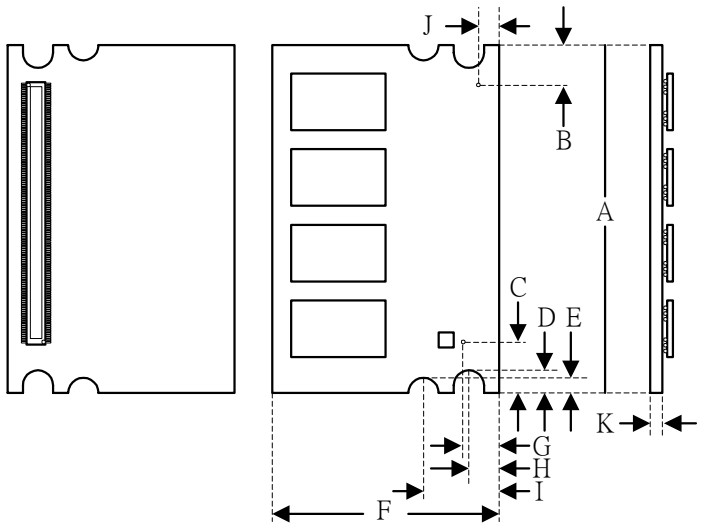
The TS32MMQ64V5M is a 32M x 64bits DDR2-533 Micro-DIMM. The TS32MMQ64V5M consists of 4pcs 32Mx16bits DDR2 SDRAMs in 84 ball FBGA packages and a 2048 bits serial EEPROM on printed circuit board with a 214Pin connector. The TS32MMQ64V5M is available as non-ECC module in 1-row 32Mx64 organization and is intended for mounting into 214-pin mezzanine connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- JEDEC standard 1.8V ± 0.1V Power supply
- VDDQ=1.8V ± 0.1V
- Max clock Freq: 267MHZ; 533Mb/s/Pin.
- Posted CAS
- Programmable CAS Latency: 3,4,5
- Programmable Additive Latency :0, 1,2,3 and 4
- Write Latency (WL) = Read Latency (RL)-1
- Burst Length: 4,8(Interleave/nibble sequential)
- Programmable sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- MRS cycle with address key programs.
- On Die Termination
- Refresh and Self Refresh
  Average Refresh Period 7.8us at lower then TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
- Serial presence detect with EEPROM

Placement



PCB: 09-2240

Dimensions

Side	Millimeters	Inches
A	54.0±0.15	2.126±0.006
B	4.725	0.186
C	5.525	0.218
D	2.3	0.09
E	1.15	0.045
F	30.0±0.15	1.18±0.006
G	3.525	0.139
H	2.9	0.114
I	7.2	0.283
J	2.275	0.09
K	0.8±0.075	0.031±0.003

(Refer Placement)

Pin Identification

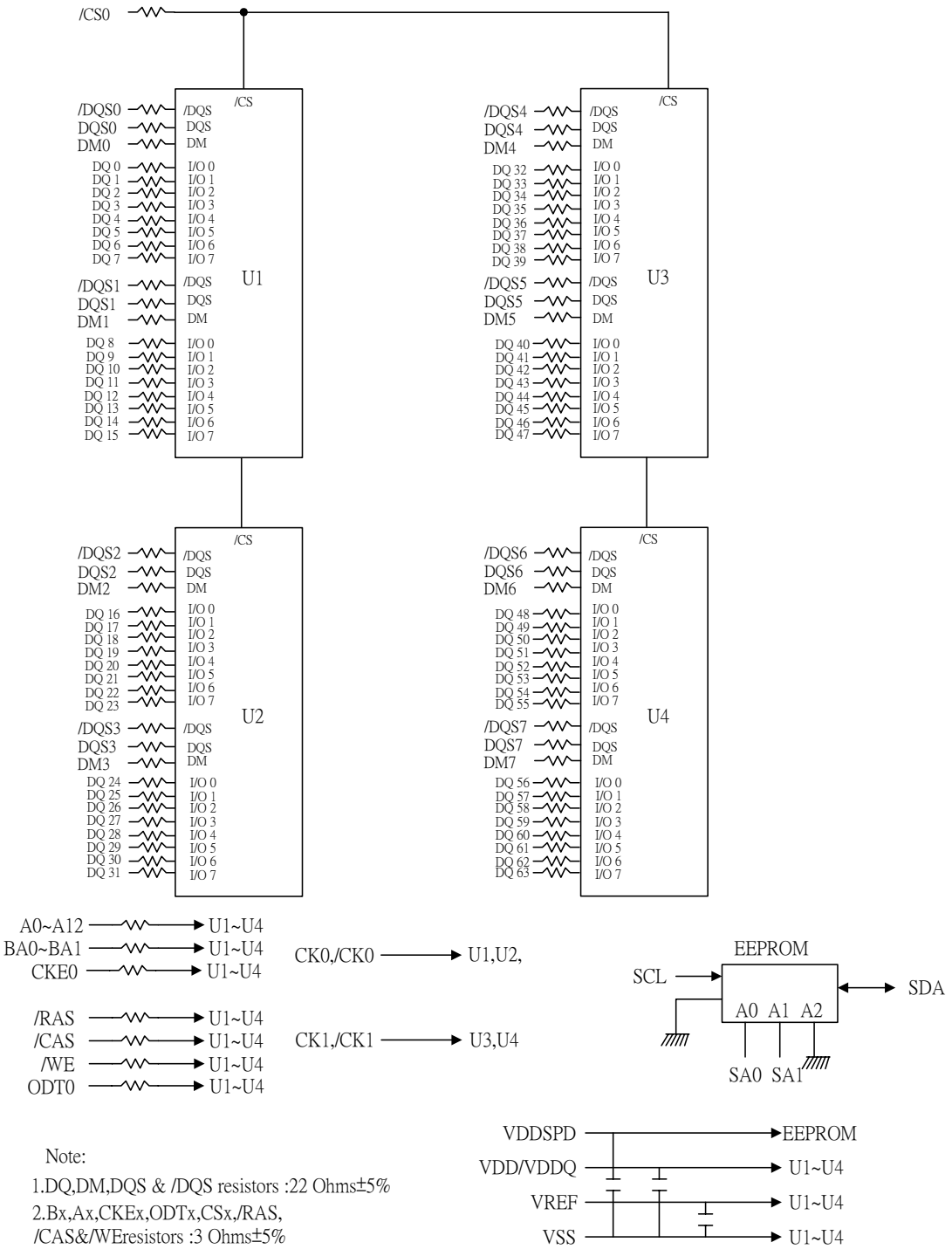
Symbol	Function
A0~A12, BA0~BA2	Address input
DQ0~DQ63	Data Input / Output.
DQS0~DQS7	Data strobe
/DQS0~/DQS7	Differential Data strobe
CK0, /CK0 CK1, /CK1	Clock Input.
CKE0	Clock Enable Input.
ODT0,	On-die termination control line
/CS0	Chip Select Input.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM7	Data-in Mask
VDD	+1.8 Voltage power supply
VDDQ	+1.8 Voltage Power Supply for DQS
VREF	Power Supply for Reference
VDDSPD	Serial EEPROM Positive Power Supply
SA0~SA1	Address select for EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
VSS	Ground
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREF	108	VSS	37	VSS	144	VSS	73	DQ34	180	DQ39
02	VSS	109	DQ4	38	DQ26	145	NC	74	DQ35	181	VSS
03	DQ0	110	DQ5	39	DQ27	146	VDD	75	VSS	182	DQ44
04	DQ1	111	VSS	40	VSS	147	CKE1	76	DQ40	183	DQ45
05	VSS	112	DM0	41	NC	148	NC	77	DQ41	184	VSS
06	/DQS0	113	VSS	42	VDD	149	VDD	78	VSS	185	/DQS5
07	DQS0	114	DQ6	43	CKE0	150	NC	79	DM5	186	DQS5
08	VSS	115	DQ7	44	NC	151	NC	80	VSS	187	VSS
09	DQ2	116	VSS	45	VDD	152	VDD	81	DQ42	188	DQ46
10	DQ3	117	DQ12	46	BA2	153	A12	82	DQ43	189	DQ47
11	VSS	118	DQ13	47	A11	154	A9	83	VSS	190	VSS
12	DQ8	119	VSS	48	A7	155	A8	84	DQ48	191	DQ52
13	DQ9	120	DM1	49	VDD	156	VDD	85	DQ49	192	DQ53
14	VSS	121	VSS	50	A5	157	A6	86	VSS	193	VSS
15	NC	122	CK0	51	A4	158	A3	87	NC	194	CK1
16	NC	123	/CK0	52	A2	159	A1	88	NC	195	/CK1
17	VSS	124	VSS	53	VDD	160	VDD	89	VSS	196	VSS
18	/DQS1	125	DQ14	54	A10	161	A0	90	DM6	197	/DQS6
19	DQS1	126	DQ15	55	BA0	162	BA1	91	VSS	198	DQS6
20	VSS	127	VSS	56	/WE	163	/RAS	92	DQ50	199	VSS
21	DQ10	128	DQ20	57	VDD	164	VDD	93	DQ51	200	DQ54
22	DQ11	129	DQ21	58	NC	165	/CS0	94	VSS	201	DQ55
23	VSS	130	VSS	59	NC	166	PDT0	95	DQ56	202	VSS
24	DQ16	131	DM2	60	/CAS	167	NC	96	DQ57	203	DQ60
25	DQ17	132	VSS	61	VDD	168	VDD	97	VSS	204	DQ61
26	VSS	133	DQ22	62	/CS1	169	NC	98	/DQS7	205	VSS
27	/DQS2	134	DQ23	63	ODT1	170	NC	99	DQS7	206	DM7
28	DQS2	135	VSS	64	VDD	171	VDD	100	VSS	207	VSS
29	VSS	136	DQ28	65	NC	172	NC	101	DQ58	208	DQ62
30	DQ18	137	DQ29	66	VSS	173	VSS	102	DQ59	209	DQ63
31	DQ19	138	VSS	67	DQ32	174	DQ36	103	VSS	210	VSS
32	VSS	139	/DQS3	68	DQ33	175	DQ37	104	SDA	211	SA0
33	DQ24	140	DQS3	69	VSS	176	VSS	105	SCL	212	NC
34	DQ25	141	VSS	70	/DQS4	177	DM4	106	NC	213	SA1
35	VSS	142	DQ30	71	DQS4	178	VSS	107	VDDSPD	214	NC
36	DM3	143	DQ31	72	VSS	179	DQ38				

* Please refer Block Diagram

Block Diagram



Note:

1.DQ,DM,DQS & /DQS resistors :22 Ohms±5%

2.Bx,Ax,CKEx,ODTx,CSx,/RAS, /CAS&/WEresistors :3 Ohms±5%

This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on V_{DD} relative to Vss	VDD	-1.0 ~ 2.3	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.5 ~ 2.3	V	1
Voltage on V_{DDL} pin relative to Vss	VDDL	-0.5 ~ 2.3	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ 2.3	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2
Mean time between failure	MTBF	Reserved	year	
Temperature Humidity Burning	THB	Reserved	°C-%	
Temperature Cycling Test	TC	Reserved	°C	

Note:
1.Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2.Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions (SSTL –1.8)

Parameter	Symbol	Rating			Unit	Notes
		Min	Typ.	Max		
Supply voltage	VDD	1.7	1.8	1.9	V	
Supply voltage for DLL	VDDL	1.7	1.8	1.9	V	4
Supply voltage for Output	VDDQ	1.7	1.8	1.9	V	4
I/O Reference voltage	VREF	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	1,2
I/O Termination voltage	VTT	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
DC Input logic high	$V_{IH(DC)}$	V_{REF}+0.125	-	V_{DDQ}+0.3	V	
DC Input logic low	$V_{IL(DC)}$	-0.3	-	V_{REF}-0.125	V	

Note:
There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.
1.The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2.Peak to peak AC noise on VREF may not exceed +/-2% VREF (DC).
3.VTT of transmitting device must track VREF of receiving device.
4.AC parameters are measured with VDD, VDDQ and VDDDL tied together.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 95	°C	1,2,3

Note:
1.Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 0 - 85°C, operation temperature range are the temperature which all DRAM specification will be supported.
3. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

IDD Specification parameters Definition

(IDD values are for full operating range of voltage and Temperature)

Parameter		Symbol	Max.	Unit	Note
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD0	480	mA	
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		IDD1	520	mA	
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2P	32	mA	
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2Q	100	mA	
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD2N	120	mA	
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	IDD3P-F	120	mA	
	Slow PDN Exit MRS(12) = 1mA	IDD3P-S	60		
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD3N	280	mA	
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		IDD4R	920	mA	
Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R		IDD4W	820	mA	
Burst Auto refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD5B	780	mA	
Self refresh current; CK and CK\ at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		IDD6	22	mA	
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK =tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during Deselects; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions		IDD7	1,560	mA	

Note: 1. Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading capacitor.

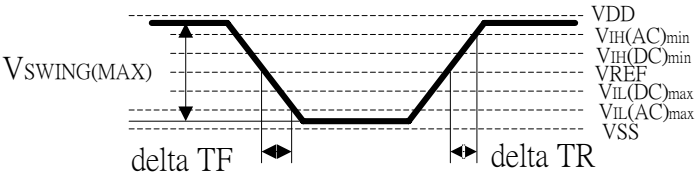
Input AC Logic Level

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.250		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.250	V	

AC Input Test Condition

Condition	Symbol	Value	Unit	Note
Input reference voltage	VREF	0.5*VDDQ	V	1
Input signal maximum peak to peak swing	VSWING(MAX)	1.0	V	1
Input signal minimum slew rate	SLEW	1.0	V/ns	2,3

Note:
1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(AC) min for rising edges and the range from VREF to VIL(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(AC) to VIH(AC) on the positive transitions and VIH(AC) to VIL(AC) on the negative transitions.



$$\text{Falling Slew} = \frac{V_{REF} - V_{IL}(AC)_{max}}{\text{delta TF}} \qquad \text{Rising Slew} = \frac{V_{IH}(AC)_{min} - V_{REF}}{\text{delta TR}}$$

AC Input Test Signal Waveform

Input/Output Capacitance (V_{DD} = 1.8V, V_{DDQ} = 1.8V, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input capacitance (CK0 and /CK0)	CCK0	-	24	pF
Input capacitance (CK1 and /CK1)	CCK1	-	24	pF
Input capacitance (CKE and /CS)	CI_1	-	34	pF
Input capacitance (A0~A13, BA0~BA2, /RAS, /CAS, /WE)	CI_2	-	34	pF
Input capacitance (DQ, DM, DQS, /DQS)	CIO	-	6	pF

Note: DM is internally loaded to match DQ and DQS identically.

Timing Parameters & Specifications

(These AC characteristics were tested on the Component)

Parameter	Symbol	Min	Max	Unit	Note
DQ output access time from CK & /CK	tAC	-500	+500	ps	
DQS output access time from CK & /CK	tDQSCK	-450	+450	ps	
CK high-level width	tCH	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	tCK	
CK half period	tHP	min(tCL,tCH)	X	ps	
Clock cycle time, CL=x	tCK	3750	8000	ps	
DQ and DM input hold time	tDH	225	x	ps	
DQ and DM input setup time	tDS	100	X	ps	
Control & Address input pulse width for each input	tIPW	0.6	x	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	X	tCK	
Data-out high-impedance time from CK/CK	tHZ	X	tAC max	ps	
DQS low-impedance time from CK/CK	tLZ(DQS)	tAC min	tAC max	ps	
DQ low-impedance time from CK/CK	tLZ(DQ)	2*tAC min	TAC max	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	X	300	ps	
DQ hold skew factor	tQHS	X	400	ps	
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	X	ps	
Write command to first DQS latching transition	tDQSS	WL-0.25	WL+0.25	tCK	
DQS input high pulse width	tDQSH	0.35	X	tCK	
DQS input low pulse width	tDQSL	0.35	X	tCK	
DQS falling edge to CK setup time	tDSS	0.2	X	tCK	
DQS falling edge hold time from CK	tDSH	0.2	X	tCK	
Mode register set command cycle time	tMRD	2	X	tCK	
Write postamble	tWPST	0.4	0.6	tCK	
Write preamble	tWPRE	0.35	X	tCK	
Address and control input hold time	tIH	375	X	ps	
Address and control input setup time	tIS	250	X	ps	
Read preamble	tRPRE	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	tCK	
Active to active command period for 1KB page size products	tRRD	7.5	X	ns	
Active to active command period for 2KB page size products	tRRD	10	X	ns	
Four Activate Window for 1KB page size products	tFAW	37.5		ns	
Four Activate Window for 2KB page size products	tFAW	50		ns	

/CAS to /CAS command delay	tCCD	2		tCK	
Write recovery time	tWR	15	X	ns	
Auto precharge write recovery + precharge time	tDAL	tWR+tRP	X	tCK	
Internal write to read command delay	tWTR	7.5	X	ns	
Internal read to precharge command delay	tRTP	7.5		ns	
Exit self refresh to a non-read command	tXSNR	tRFC + 10		ns	
Exit self refresh to a read command	tXSRD	200		tCK	
Exit precharge power down to any non-read command	tXP	2	X	tCK	
Exit active power down to read command	tXARD	2	X	tCK	
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL		tCK	
CKE minimum pulse width (high and low pulse width)	tCKE	3		tCK	
ODT turn-on delay	tAOND	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max)+1	ns	
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	2tCK+ tAC(max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max)+ 0.6	ns	
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3		tCK	
ODT power down exit latency	tAXPD	8		tCK	
OCD drive mode output delay	tOIT	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH		ns	

SERIAL PRESENCE DETECT SPECIFICATION

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	# of Serial PD Bytes written during module production	128bytes	80
1	Total # of Bytes of S.P.D Memory Device	256bytes	08
2	Fundamental Memory Type	DDR2 SDRAM	08
3	# of Row Addresses on this Assembly	14	0D
4	# of Column Addresses on this Assembly	10	0A
5	# of Module Rows on this Assembly	1 ROW, Planar, 30.0mm	60
6	Data Width of this Assembly	64bits	40
7	Reserved	-	00
8	VDDQ and Interface Standard of this Assembly	SSTL 1.8V	05
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	3.75ns	3D
10	DDR2 SDRAM Access time from clock at CL=X	±0.5ns	50
11	DIMM configuration type (non-parity, Parity, ECC)	Non ECC	00
12	Refresh Rate	7.8us	82
13	Primary DDR2 SDRAM Width	X8	10
14	Error Checking DDR2 SDRAM Width	N/A	00
15	Reserved	-	00
16	DDR2 SDRAM device attributes: Burst lengths supported	4,8	0C
17	DDR2 SDRAM device attributes: # of banks on each DDR2 SDRAM device	4 banks	04
18	DDR2 SDRAM device attributes:CAS Latency supported	5,4,3	38
19	Reserved	-	00
20	DIMM type information	Micro-DIMM	08
21	DDR2 SDRAM Module Attributes	Analysis probe not installed, FET switch external not enable	00
22	DDR2 SDRAM Device Attributes: General	Supports weak driver	01
23	DDR2 SDRAM Cycle Time CL=X-1	3.75ns	3D
24	DDR SDRAM Access from Clock CL=X-1	±0.5ns	50
25	DDR SDRAM Cycle Time CL=X-2	5.0ns	50
26	DDR SDRAM Access from Clock CL=X-2	±0.6ns	60
27	Minimum Row Precharge Time (tRP)	15ns	3C
28	Minimum Row Active to Row Activate delay (tRRD)	1.0ns	28
29	Minimum RAS to CAS Delay (tRCD)	15ns	3C
30	Minimum active to Precharge time (tRAS)	40ns	2D
31	Module ROW density	256MB	40
32	Command and address setup time before clock(=tIS)	0.25ns	25
33	Command and address hold time after clock(=tIH)	0.37ns	37
34	Data input setup time before strobe(=tDS)	0.10ns	10
35	Data input hold time after strobe(=tDH)	0.22ns	22
36	Write recovery time(=tWR)	15ns	3C

37	Internal write to read command delay(=tWTR)	7.5ns	1E
38	Internal read to precharge command delay(=tRTP)	7.5ns	1E
39	Memory analysis probe characteristics	-	00
40	Reserved	-	00
41	DDR SDRAM Minimum Active to Active/Auto Refresh Time(tRC)	55ns	3C
42	DDR SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	105ns	69
43	DDR SDRAM Maximum Device Cycle Time (tCK max)	8ns	80
44	DDR SDRAM DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)	0.3ns	1E
45	DDR SDRAM Read Data Hold Skew Factor (tQHS)	0.4ns	28
46	PLL Relock Time	-	00
47	$T_{CASE.max}$ Delta / Δ T_{4R4W} Delta	-	53
48	Psi(T-A) DRAM	-	72
49	Δ T_0 (DT0)	-	52
50	Δ T_{2N} (DT2N, UDIMM) or Δ T_{2Q} (DT2Q, RDIMM)	-	2B
51	Δ T_{2P} (DT2P)	-	1D
52	Δ T_{3N} (DT3N)	-	1D
53	Δ $T_{3P.fast}$ (DT3P fast)	-	23
54	Δ $T_{3P.slow}$ (DT3P slow)	-	16
55	Δ T_{4R} (DT4R) / Δ $T_{4R4W\ S}$ Sign (DT4R4W)	-	36
56	Δ T_{5B} (DT5B)	-	1C
57	Δ T_7 (DT7)	-	30
58~61	Superset Information	-	00
62	SPD Data Revision Code	REV 1.1	11
63	Checksum for Bytes 0-62	53	53
64-71	Manufacturers JEDEC ID	Transcend	7F, 4F
72	Manufacturing Location	T	54
73-90	Manufacturers Part Number	TS32MMQ64V5M	54 53 33 32 4D 4D 51 36 34 56 35 4D 20 20 20 20 20 20
91-92	Revision Code	-	-
93-94	Manufacturing Date	By Manufacturer	Variable
95-98	Assembly Serial Number	By Manufacturer	Variable
99-127	Manufacturer Specific Data	-	-
128~255	Open for customer use	Undefined	-